# Digital Logic Gates Constructed from Two NPN Transistors (aka *What’s Inside These*  ? )

|  |  |  |
| --- | --- | --- |
| **CONFIGURATION** | **TWO NPNs in SERIES** | **TWO NPNs in PARALLEL** |
| **Pull DOWNResistorOutput** | BinaryANDLogic.gifName: **AND**Symbol: and-gate-hi.png

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

 | Name: \_\_\_\_\_\_\_Symbol:

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

 |
| **Pull UPResistorOutput** | Name: \_\_\_\_\_\_Symbol:

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

 | Name:\_\_\_\_\_\_Symbol:

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

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