# Digital Logic Gates Constructed from Two NPN Transistors (aka *What’s Inside These* ? )

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| **CONFIGURATION** | **TWO NPNs in SERIES** | **TWO NPNs in PARALLEL** |
| **Pull DOWN Resistor Output** | BinaryANDLogic.gif  Name: **AND**  Symbol:  and-gate-hi.png   |  |  |  | | --- | --- | --- | | **A** | **B** | **Y** | | 0 | 0 | 0 | | 0 | 1 | 0 | | 1 | 0 | 0 | | 1 | 1 | 1 | | Name: \_\_\_\_\_\_\_  Symbol:     |  |  |  | | --- | --- | --- | | **A** | **B** | **Y** | | 0 | 0 |  | | 0 | 1 |  | | 1 | 0 |  | | 1 | 1 |  | |
| **Pull UP Resistor Output** | Name: \_\_\_\_\_\_  Symbol:   |  |  |  | | --- | --- | --- | | **A** | **B** | **Y** | | 0 | 0 |  | | 0 | 1 |  | | 1 | 0 |  | | 1 | 1 |  | | Name:\_\_\_\_\_\_  Symbol:   |  |  |  | | --- | --- | --- | | **A** | **B** | **Y** | | 0 | 0 |  | | 0 | 1 |  | | 1 | 0 |  | | 1 | 1 |  | |