### INSTRUCTIONS TO JR. ACES

1. You have sufficient time to complete the entire task if you remain calm and follow the instructions.
2. An electronic copy of this exam can be found attached to the most recent email in our TEL3M First Class subject conference. Download it and place in on your Desktop.
3. Be patient, read over all 4 pages of this exam to appreciate the full set of requirements.
4. This exam counts for 30% of your final mark in this course.
5. Please write your name in the space provide in the header.
6. Please keep your work secure at all times.
7. In addition to your toolkit, the supplemental parts kit (page 2) contains the necessary parts to assemble the circuit whose schematic appears below. Handle the components with care as replacement parts are not available.
8. This is an *open* examination in that you are free to use your Evil *Genius Workbook* and the *internet* for reference purposes *only*. It remains inappropriate to communicate with anyone.
9. When you finish (or when time expires), submit your ER to handin (Subject: **Final Exam**) and remain seated and quiet until ALL students have had their circuits collected.

This examination requires you to modify your most recent circuit

**The NAND Gate Oscillator**

and document the results in your *Engineering Report*.

### EVALUATION

You are required to develop a working prototype of the circuit described below and document the outcome in your *Engineering Report*. Credit will be awarded as follows.

**20 Marks. Prototype** (*Knowledge, Application, Thinking, Inquiry, Problem Solving*)

15 a) **Works.**  Credit will be awarded proportionally to the extent your circuit functions as expected.

5 b) **Build Quality**. Build quality includes layout/arrangement of parts.

**10 Marks. Engineering Report** (*Communication*)

7 a) **Content**. All required elements are included. See below.

3 b) **Presentation Skill**. These include formatting features (*we’ve discussed all year*) such as the *proper use of styles, pagination, headers & footers, page numbering, image positioning, hyperlinks, table formatting, spelling, grammar, creativity*, etc.

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| **MR. D’ARCY’S USE ONLY** |

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| --- | --- | --- | --- | --- |
| **PROTOTYPE** | | **ENGINEERING REPORT** | | **TOTAL** |
| **WORKS** | **BUILD QUALITY** | **CONTENT** | **PRESENTATION** |
| **/10** | **/5** | **/10** | **/5** | **/30** |

**SUPPLEMENTAL PARTS KIT**

Your supplemental parts kit contains the additional components required to complete the modification of your *NAND Gate Oscillator* prototype.

|  |  |  |
| --- | --- | --- |
| **QUANTITY** | **COMPONENT** | **IMAGE** |
| 1 | Hookup Wire Kit | WireKit.jpg |
| 1 | **CMOS 4026** decade counter and 7-segment display driver | 4017.jpg |
| 1 | 9V Battery | 9VProcell.jpg |
| 1 | 9V Battery Clip | 9VBatteryClip.jpg |

### THE PROTOTYPE

1. Currently, the output of your *NAND Gate Oscillator* circuit generates a clock signal (alternating High/Low) on pin 10 of your **4011** with a frequency determined by RC2 and over a period of time determined by RC1. This clock signal is used as input to pin 15 of a **4516 Up/Down counter**. The **4516** uses the clock pulse to maintain an internal 4-bit counter, the state of which it presents on output pins 6, 11, 14, and 2. These signals are currently being used as input to a **4511 BCD 7-segment decoder** to drive a 7-segment display in which the 10 decimal digits appear before going dark while the input provides values from 10 to 16.
2. To achieve a more compact circuit, you have been provided with s **CMOS 4026** decade counter and  
   7-segment display driver IC. Since this semiconductor chip combines the function of the **4510** and **4511** you can consolidate your circuit by removing two ICs and replacing it with one.

**THE TASK**

1. **View** this video. It is the same video that was used for last year’s exam since the output is the same.

<http://www.youtube.com/watch?v=4VUk0ijn5wk>

1. **Research the 4026.** Use the internet to research the pin mapping and wiring details of the 4026 decade counter and 7-segment display driver.
2. **Prototype**. With your power source disconnected, modify your current circuit by replacing the **4516** and **4511** with the **4026**. Be sure to follow good breadboard layout design principles. This includes removing all unnecessary wires leftover from the removal of the **4516** and **4511.**
3. **Power.** Plug in your 9V battery and test your circuit. Debug as required.
4. **Engineering Report**. At the top of the first new page after **Project 5. The Basic Digital Logic Gates**, add the entry, **Project 6. Final Exam** in Heading 1 style.
5. Within Heading 3 style subheadings, include the following
   1. **Purpose**. In your own words explaining what this circuit does.
   2. **Parts List**. Create a parts list from the information given.
   3. **Procedure**. Describe the process you undertook to complete this circuit. Supplement your discussion with a good image of the 4026 decade counter and  
      7-segment display driver, fully explaining the rationale for its incorporation and its contribution to your circuit.
   4. **Photos**. Using your laptop, obtain a photo of your working circuit and insert it into your ER, formatting it as you have become accustomed.
6. Save your ER and attach it to an email to handin under the Subject Line: **Final Exam**.
7. Remain seated until all circuits have been collected.

**----End of Examination----**

This concludes our introduction to electrical engineering.  
 Hopefully, I’ll see many of you in the Grade 11 course, TEI3M.

You can leave all your tools at home next week with the exception of your laptop.