### INSTRUCTIONS TO JR. ACES

1. You have sufficient time to complete the entire task if you remain calm and follow the instructions.
2. A copy of this exam can be found attached to the most recent email in our TEL3M First Class subject conference. Download it and place in on your Desktop.
3. Be patient, read over all 4 pages of this exam to appreciate the full set of requirements.
4. This exam counts for 30% of your final mark in this course.
5. Please write your name in the space provide in the header.
6. Please keep your work secure at all times.
7. In addition to your toolkit, the supplemental parts kit (page 2) contains the necessary parts to assemble the circuit whose schematic appears below. Handle the components with care as requests for replacement parts will reduce your score.
8. This is an *open* examination in that you are free to use your Evil *Genius Workbook* and the *internet* for reference purposes *only*. You are not to abuse this privilege by communicating with others.
9. When you finish (or when time expires), submit your ER to handin (Subject: **Final Exam**) and remain seated until all students have had their circuits collected.

This examination requires you to extend your most recent circuit

**The NAND Gate Oscillator**

and document the results in your *Engineering Report*.

### EVALUATION

You are required to develop a working prototype of the circuit described below and document the outcome in your *Engineering Report*. Credit will be awarded as follows.

**20 Marks. Prototype** (*Knowledge, Application, Thinking, Inquiry, Problem Solving*)

15 a) **Works?** Credit will be awarded proportionally to the extent your circuit functions as expected.

5 b) **Build Quality**. Build quality includes layout/arrangement of parts.

**10 Marks. Engineering Report** (*Communication*)

7 a) **Content**. All required elements are included. See below.

3 b) **Presentation Skill**. These include formatting features (*we’ve discussed all year*) such as the *proper use of styles, pagination, headers & footers, page numbering, image positioning, hyperlinks, table formatting, spelling, grammar, creativity*, etc.

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| --- |
| **MR. D’ARCY’S USE ONLY** |

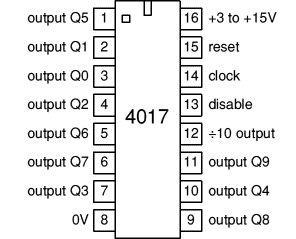
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **PROTOTYPE** | | **ENGINEERING REPORT** | | **TOTAL** |
| **WORKS?** | **BUILD QUALITY** | **CONTENT** | **PRESENTATION SKILL** |
| **/15** | **/5** | **/7** | **/3** | **/30** |

**SUPPLEMENTAL PARTS KIT**

Your supplemental parts kit contains the additional components required to complete the extension of your *NAND Gate Oscillator* prototype.

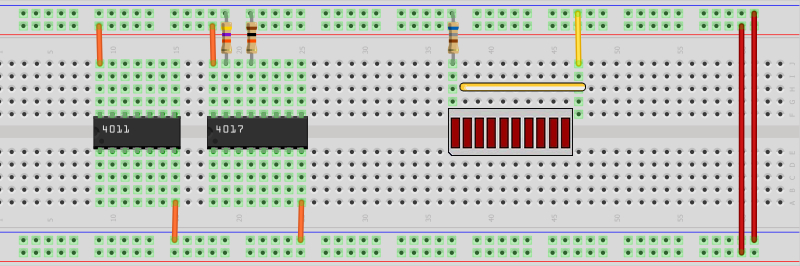
|  |  |  |
| --- | --- | --- |
| **QUANTITY** | **COMPONENT** | **IMAGE** |
| 1 | Hookup Wire Kit | WireKit.jpg |
| 1 | CMOS 4017 Decade (Walking Ring) Counter | 4017.jpg |
| 1 | 10 Segment LED Bargraph Reference bevel highlighted (anode side) | 09Bargraph3 |
| 1 | 10-pin 680Ω Resistor Network (bussed) | RN10SIPB.jpg |
| 1 | 47k Ω 1/4W Fixed Resistor | 47K.jpg |
| 1 | 10k Ω 1/4W Fixed Resistor | 10K.jpg |
| 1 | 680 Ω 1/4W Fixed Resistor | 680.jpg |

### THE PROTOTYPE

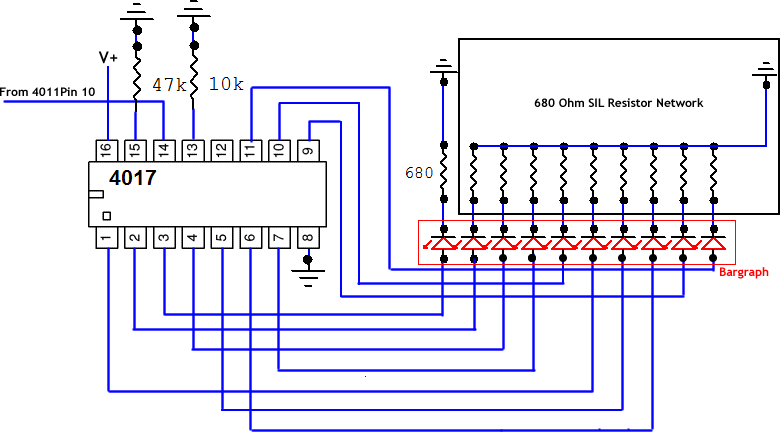
1. Currently, the output of your *NAND Gate Oscillator* circuit generates a clock signal (alternating H/L) on pin 10 of your 4011 for a period of time determined by RC1. You currently flash a single LED to monitor this signal.
2. In this examination, you will use the signal to propel a sequence of **10 LEDs** packaged in what is known as a bar graph.
3. To convert this *single* pulse into a sequence of 10 separate voltage sources required for the 10 LEDs in the bar graph, you will incorporate a specialized IC known as the **4017 Walking Ring Decade Counter**. (*you have one in your toolbox but I’ve given you an extra one in case you can’t find it*)
4. A pin diagram of the 4017 **16**-pin IC appears to the right and, for our immediate purpose, functions as follows. It has one main input (pin 14-clock signal) and 10 possible outputs (pins 1 through 7, and pins 9 through 11). **Note: they’re not in order!** Each clock signal pulse received at pin 14 causes each of its 10 output pins to go High in sequence, with only one pin High at a time. The sequence is *cyclical*, meaning that after pin 11 **(output Q9)** goes High, pin 3 **(output Q0)** goes High., then pin 2 **(output Q1)**, and so on
5. If each of these pins is connected to the correct anode lead of each LED in the bar graph, we should see the LED pattern that appears in this video sequence.

<http://www.youtube.com/watch?v=W975ZL-cQvc>

**GENERAL POSITIONING OF THE MAJOR COMPONENTS**



**THE SCHEMATIC**



**THE TASK**

1. **Prototype**. Assemble the prototype as described above to obtain the output highlighted in the video. Be sure to follow good layout design principles.
2. **Engineering Report**. At the top of the first new page after Activity 5, add the entry, **Activity 6. Final Exam** in Heading 1 style.
3. Within Heading 3 style subheadings, include the following
   1. **Purpose**. In your own words explaining what this circuit does.
   2. **Procedure**. Describe the process you undertook to complete this circuit.
   3. **Parts List**. Obtain a copy of the parts list from this document and insert it into your ER.
   4. **General Positioning of Major Components**. Obtain a copy of the *General Positioning* image above and insert it into your ER.
   5. **Schematic**. Obtain a copy of the circuit schematic above and insert it into your ER.
   6. **Photo**. Using your laptop, obtain a photo of your working circuit and insert it into your ER, formatting it as you have become accustomed to (200 px wide, right-aligned with a 1-pixel border)
4. Save your ER and attach it to an email to handin under the Subject Line: **Final Exam**.

**----End of Examination----**