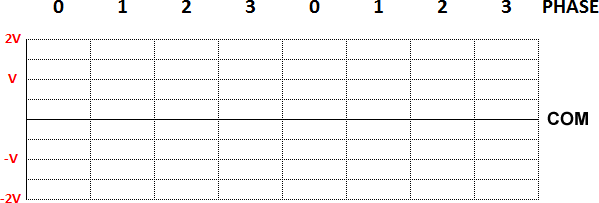
### 1. TLD: Two Port

A four-state logic array, with potential denoted by **V**, is presented cyclically on two ports, **A** and **B**. The sequence starts with **A** and **B** indexed as shown, with each advancing on every phase. All resistors are 10kΩ.

a) For the schematic provided, complete the table, below right.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ThreeLevelTwoPort.png | |  |  |  |  | | --- | --- | --- | --- | | **PHASE** | **A** | **B** | **COM** | | **0** |  |  |  | | **1** |  |  |  | | **2** |  |  |  | | **3** |  |  |  | | **0** |  |  |  | | **1** |  |  |  | | **2** |  |  |  | | **3** |  |  |  | |

b) Graph **COM**.



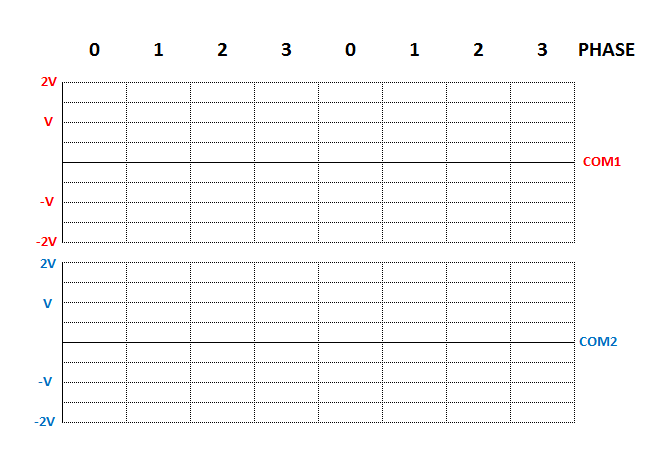
### 2. TLD: Three Port

The same four-state logic array is presented, cyclically, now on three ports, **A**, **B**, and **C**, with starting indices as shown.

a) For the schematic provided, complete the table, below right.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ThreeLevelThreePort.png | |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | **PHASE** | **A** | **B** | **C** | **COM1** | **COM2** | | **0** |  |  |  |  |  | | **1** |  |  |  |  |  | | **2** |  |  |  |  |  | | **3** |  |  |  |  |  | | **0** |  |  |  |  |  | | **1** |  |  |  |  |  | | **2** |  |  |  |  |  | | **3** |  |  |  |  |  | |

b) Graph the **COM1** and **COM2** output signals on their respective charts.



c) Are the two outputs in phase? If yes, by how many degrees are they out of phase?