Pierce-Gate Crystal Oscillator, an introduction

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Introduction

The most common gate oscillator in use today is by far the Pierce-Gate shown in Figure 1. Its popularity stems from the fact that the digital inverter, U1, is usually included in the microprocessor or ASIC the designer selects. In effect, the oscillator cell U1 is free!

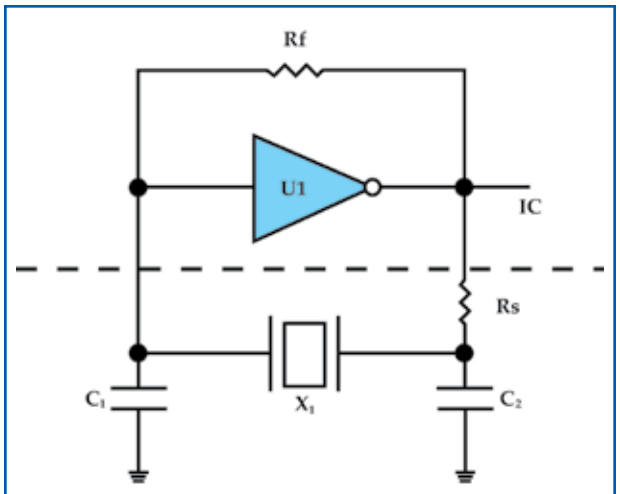

Figure 1: Fundamental Mode Isolated Pierce- Gate Oscillator

Most designers are familiar with the Pierce-Gate topology, but few really understand how it functions, let alone how to properly design it. As a common practice, most don't even pay too much attention to the oscillator in their design until it does not function properly, usually already released to production. This should not be case. Many systems or projects have been delayed in their deployment because of a twenty-five cent crystal not working as intended. The oscillator should receive its proper amount of attention during the design phase, well before the manufacturing phase. The designer would then avoid the nightmare scenario of product being returned from the field.

We will analyze how the Pierce-Gate oscillator functions by breaking it down to its components. (A much more rigorous analysis is beyond the scope of this paper.) However, the simple analysis will suffice to convey the key points of Pierce-Gate Oscillator operation. In addition, we'll present a simple design problem to teach how to derive at the Pierce-gate initial values.

The Basic Pierce-Gate Oscillator

We can use the Barkhausen criteria to explain how the Pierce-gate topology works. The criteria states the following:

a. The product of the gains around the loop must be equal to or greater than one at the desired frequency of oscillation.
b. The phase shift around the loop must be zero or any integer multiple of 2π (360°).

Figure 2 shows the phase shift analysis for the Pierce-gate. If U1 provides -180° phase shift, an additional -180° by the rest of external components is required to satisfy the Barkhausen criteria. The phase shift will automatically adjust itself to be exactly 360° around the loop in order to keep oscillating. If U1 provides -185° phase shift, the rest of the components will automatically provide -175° phase shift in a properly working design.

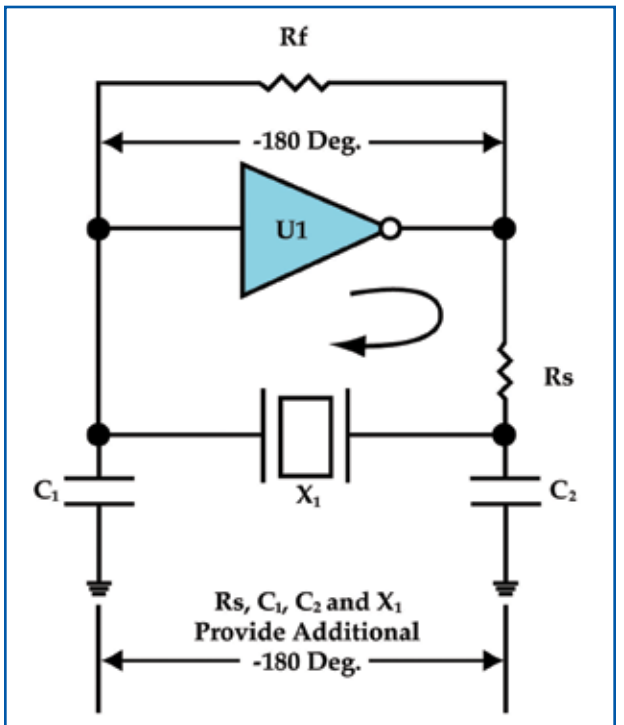

Figure 2: Pierce-Gate Phase Shift Analysis

The gain around the loop is a function of gm (transconductance) of the inverter and reactance of C1 and C2 (Xc1, Xc2) and Rs. Without Rs in the loop, the gain in terms of negative resistance is:

$$\text{negative resistance} = -gmX_{C1}X_{C2} \quad \text{Eq. 1}$$

Since $X_c = 1/jwc$, the negative resistance (gain) goes up as the capacitors C1 and C2 are reduced. Hence, decrease C1 and C2 to increase the gain around the loop. It is easy to see that Rs decreases the gain around the loop as its value is increased. A starting value for Rs is to set it equal to the reactance of XC2.

Feedback Resistor Rf

The feedback resistor Rf is there to linearize the digital CMOS inverter. Rf accomplishes this feat by charging the inverter's input capacitance, including C1 from the output of the inverter. In other words, the feedback resistor transforms a logic gate into an analog amplifier. Pretty neat trick by simply adding a single resistor.

Generally the feedback resistor is included with the micro or ASIC. Use the following procedure to determine if the feedback resistor is integrated in the IC:

- With no external components connected (C1, C2 and X1), measure the voltage at the input and output of the inverter.
- If the feedback resistor is inside, then the voltage at the input and output pins will be around Vcc/2.
- If the feedback resistor in not inside, then the inverter will be latched and either the input and output will be at a logic "1" or logic "0" or vice-versa.

Table 1: Typical range values for feedback resistor Rf

Frequency	Feedback Resistor Range
32.768 KHz	10~15 Meg ohms
1 MHz	5~10 Meg ohms
10 MHz	1~5 Meg ohms
20 MHz	470 K to 5 Meg ohms

The value of Rf used is frequency-dependent. The lower the frequency, the higher the value needed. Table 1 lists typical range values.

The feedback resistance Rf can be optimized in the following manner:

- With the crystal and all other components in place, determine the value of Rf which begins to pull the frequency.
- Do this by plotting frequency vs. Rf.
- Choose the value of Rf above the point where loading begins to pull the frequency.

Resistor Rs

The resistor in series with the output of the inverter, Rs, has three primary functions:

1. To isolate the output driver of the inverter from the complex impedance formed by C2, C1 and the crystal.
2. To give the designer another degree of freedom to control the drive level (expressed as power/voltage across or

current through the crystal) and/or adjust the oscillator loop gain. Rs must be used with "Tuning-Fork" (watch) crystals. Tuning-Fork crystals have a maximum drive level of 1µW maximum. Without a large Rs (greater than 10k ohms), the inverter will physically damage the crystal!

3. In conjunction with C2, Rs forms a lag network to add additional phase shift necessary especially at low frequencies, 8MHz or below. This additional phase shift is needed to reduce the jitter in the time domain or phase noise in frequency domain. Rs is sometimes not needed (especially at frequencies above 20MHz) since the output resistance of the inverter in conjunction with C2 will provide enough phase lag. However, when not be needed to phase lag it may still be needed to reduce the drive level on the crystal.

Inverter U1

The inverter U1 provides the necessary loop gain to sustain oscillation as well as approximately -180° phase shift. If the inverter is part of some ASIC or microprocessor, its manufacturer should specify the critical crystal parameters like maximum E.S.R. that will work properly under all conditions. If U1 is not part an ASIC, then the designer must carefully select an inverter with the proper gain/phase characteristics for the targeted frequency or range of frequencies. Simulation is also strongly recommended here but not necessary for a good working design. Not all digital inverters are suitable for oscillator applications. Some have too much propagation delay, even at low frequencies. On the other hand, in the past one needed an inverter with no buffer (un-buffered) for oscillators. This is not the case today since propagation delays have been reduced over the years for all modern digital inverters due to the required higher speeds of operation.

A call to the inverter manufacturer's technical support department is a good idea to get their blessing (in a sense) of your intended use as an oscillator.

Crystal X1, Capacitors C1 and C2

As mentioned above, the crystal X1, together with C1, C2 and Rs, provide an additional -180° phase lag to satisfy the Barkhausen phase shift criteria for sustaining oscillation.

In most cases C1 is set equal to C2. However, if need be, C2 can be made larger than C1 by a few standard values and set the center frequency and/or increase the loop gain. There is step-up in voltage gain that is function C2/C1.

The crystal X1 in Figure 1 needs to be

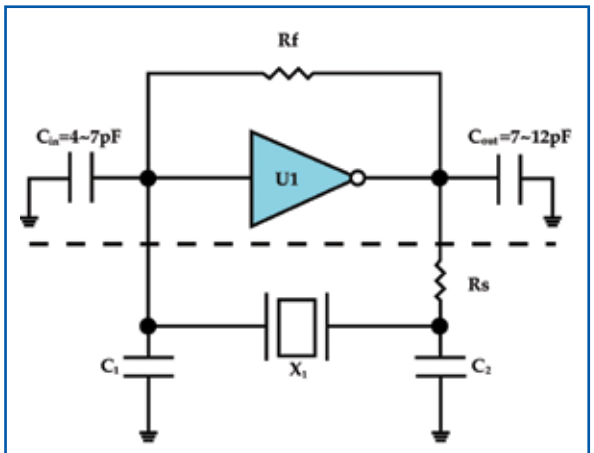

Figure 3: Pierce-Gate Showing Internal Input and Output Capacitances

a "Parallel Mode", "Fundamental" crystal. In the Pierce-gate oscillator, the crystal works in the inductive region of its reactance curve. A crystal that needs to operate in its inductive region is called a "Parallel Crystal".

Pierce-Gate Design Example

Design a 20MHz CLOCK using the Pierce-Gate topology given the following requirements:

- Frequency: 20MHz
- Frequency vs. temperature stability: +/-50 ppm
- Calibration/tolerance at +25C: +/-50 ppm
- Temperature range: -20 to +70C
- Additional requirements are:

1. low cost
2. All SMT components
3. No factory adjustment of components to meet the +/-50 ppm calibration spec.

Given are:

- The inverter gate is part of a microprocessor with Cin = 4 pF and Cout = 9 pF.
- The feedback resistor Rs is not internal as shown in Figure 1.
- The microprocessor manufacturer has already determined that a crystal with an E.S.R. = 40 ohms maximum will provide reliable operation at this frequency.

Find: C1, C2, Rs, Rf, and specify the crystal.

Solution

First, let us choose a value for Rf. This component is not critical for this design and can be within 470k~5 Meg ohms at this frequency as listed in Table 1. Therefore choose Rf = 1 Meg ohm.

The value of C1 and C2 together with Cin and Cout of the inverter (see Fig. 3) will set the load capacitance requirement on the crystal. For a clock design, you want to have the load capacitance specification of the crystal to be about the standard values of 18 or 20 pF. These are the two most common load capacitance values in the crystal industry.

The load capacitance presented to the crystal in a Pierce-Gate oscillator is,

$$C_{load} = \left\{\frac{[C_{in}+C1][C2+C_{out}]}{[C_{in}+C1+C2+C_{out}]}\right\} + \text{pcb strays (2~3 pF)}$$

Eq. 2

Most designers tend to neglect Cin and Cout either because they don't know they are there or because it is not listed in the inverter data sheet. These are significant in value compared to the external ones (C1 and C2). If Cin and Cout are not specified, then a guess value of 5 pF for each is a good start. The circuit can be later optimized by changing the starting values of C1 and C2.

In a Pierce-Gate oscillator, you want to set C2 equal to C1, or C2 greater than C1by one or two standard values. After a few iterations using Equation 2 and assuming 3 pF for the pcb strays, we can get C1 = C2 = 27 pF for our initial values.

Hence using these values we get,

$$\left\{\frac{[4\text{ pF} + 27\text{ pF}][27\text{ pF} + 9\text{ pF}]}{[4\text{ pF} + 27\text{ pF} + 27\text{ pF} + 9\text{ pF}]}\right\} + 3\text{ pF} = 19.7\text{ pF}$$

Eq. 3

Therefore specify the crystal's load capacitance as 20 pF.

The calibration or tolerance (frequency at +25°C) that we need to meet is also +/-50 ppm. Unlike the crystal's frequency vs. temperature requirement, which is controlled by the angle-of-cut of the crystal blank, the calibration can be trimmed out on the board. Our requirement, however, states no trimming/calibrating in production. In order to set the calibration spec on the crystal without trimming, we need to know how the crystal frequency changes vs. load capacitance around the 20 pF load point we chose. This is given to us by the Trim Sensitivity equation:

$$S = -\frac{C_1}{2(C_0 + C_L)^2} \times 10^{-6} \quad (\text{ppm/pF})$$

Eq. 4

Where:

C_1 = Motional capacitance of crystal
C_0 = Shunt capacitance of crystal
C_L = Load capacitance spec (20 pF in our example)

This is a nice equation since it gives us how far off frequency the oscillator will be at room temperature for every 1 pF we are away from the 20 pF load due to component variation and/or tolerance. The problem here is that the equation requires the motional and shunt capacitances, which we

don't have. However, we will complete the problem assuming a margin for the calibration. Once the crystal is ordered, request the motional parameters from the crystal manufacturer to check if the assumption that was made is good enough.

The typical commodity crystal used in this type of CLOCK has a Trim Sensitivity range of -15 to -30 ppm/pF. We will assume the high end of this range to give ourselves a +/-30 ppm margin on the calibration spec. for the crystal. Therefore, we set the crystal calibration spec to (50-30) or +/-20 ppm. Once you obtain the actual data (C_0 and C_1) from the crystal manufacturer you can check if this margin is good enough using the Trim sensitivity equation with the tolerance of the components being used. Production test data of the center frequency should be analyzed and if necessary adjust C1 and/or C2 of the Pierce oscillator.

The tighter you make the calibration spec on the crystal, the higher the price. Today, a commodity crystal is calibrated in the range of +/-25 to +/-50 ppm at room temperature. The load capacitance also directly affects the calibration spec and price. As you can see in the Trim Sensitivity equation, as C_L is made smaller, the Trim Sensitivity number goes up. Hence a 10 pF load crystal is much harder to calibrate than a 20 pF load crystal given the same design. So a bad scenario for a crystal manufacturer is a 3 pF load capacitance with a +/- 10 ppm calibration requirement.

With the value of C2 equal to 27pF, we can determine an initial value for Rs. Hence Rs is,
$Rs = 1/2\pi fC2 = 1/[(2\pi)(20MHz)(27pF)] = 398 ohms$, we set it to 390 ohms, the standard 5% value.

The crystal type needs to be an AT-cut since a BT-cut cannot meet the +/-40 ppm (+/-40 ppm for some margin) frequency stability over the temperature range of -20°C to +70°C. This gives us an initial specification minus the package of the crystal. For this we give the information of the crystal at hand to the crystal manufacturer requesting the lowest cost SMD crystal that will meet your electrical and mechanical specs.

In summary the initial design is as follows:

- Rf = 1 Meg ohm
- Rs = 390 ohms
- C1 = 27 pF
- C2 = 27 pF

The crystal specs so far are:

- Frequency: 20 MHz
- Type: AT-cut Fundamental
- Load Capacitance: 20 pF (This means "Parallel Crystal".)
- Calibration: +/- 20 ppm max. at 25°C
- Frequency Stability: +/-40 ppm max. over -20°C to +70°C
- E.S.R: 40 ohms max.
- Shunt Capacitance (C0): 7 pF max.
- Motional Capacitance (C1): not specified

At this point, the initial design is complete but needs to be validated. In general, the higher the volumes of the product, the more attention should be paid to the oscillator validation. Validation involves the following (as a minimum):

1. Measure Gain Margin
2. Perform frequency vs. temperature tests over operating supply range
3. Perform start-up at temperature extremes and supply voltage range
4. Measure the drive level through the crystal