

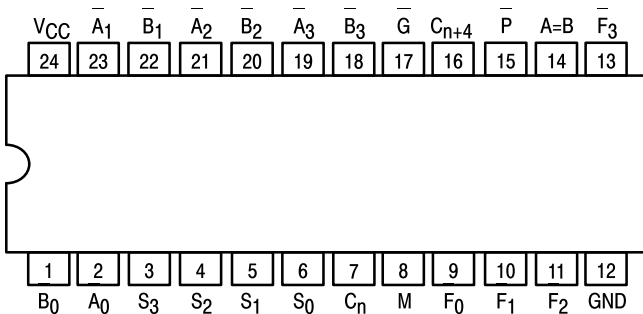


# 4-BIT ARITHMETIC LOGIC UNIT

The SN54/74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic, operations on two variables and a variety of arithmetic operations.

- Provides 16 Arithmetic Operations Add, Subtract, Compare, Double, Plus Twelve Other Arithmetic Operations
- Provides all 16 Logic Operations of Two Variables Exclusive — OR, Compare, AND, NAND, OR, NOR, Plus Ten other Logic Operations
- Full Lookahead for High Speed Arithmetic Operation on Long Words
- Input Clamp Diodes

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

$\bar{A}_0$ – $\bar{A}_3$ , $\bar{B}_0$ – $\bar{B}_3$	Operand (Active LOW) Inputs
$S_0$ – $S_3$	Function — Select Inputs
M	Mode Control Input
$C_n$	Carry Input
$F_0$ – $F_3$	Function (Active LOW) Outputs
$\bar{A} = \bar{B}$	Comparator Output
G	Carry Generator (Active LOW) Output
$\bar{P}$	Carry Propagate (Active LOW) Output
$C_{n+4}$	Carry Output

### LOADING (Note a)

	HIGH	LOW
$\bar{A}_0$ – $\bar{A}_3$ , $\bar{B}_0$ – $\bar{B}_3$	1.5 U.L.	0.75 U.L.
$S_0$ – $S_3$	2.0 U.L.	1.0 U.L.
M	0.5 U.L.	0.25 U.L.
$C_n$	2.5 U.L.	1.25 U.L.
$F_0$ – $F_3$	10 U.L.	5 (2.5) U.L.
$\bar{A} = \bar{B}$	Open Collector	5 (2.5) U.L.
G	10 U.L.	10 U.L.
$\bar{P}$	10 U.L.	5 U.L.
$C_{n+4}$	10 U.L.	5 (2.5) U.L.

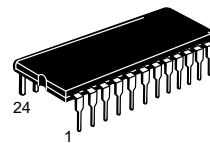
### NOTES:

- 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

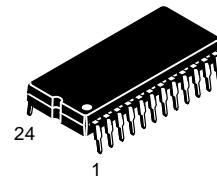
## SN54/74LS181

### 4-BIT ARITHMETIC LOGIC UNIT

#### LOW POWER SCHOTTKY



J SUFFIX  
CERAMIC  
CASE 623-05

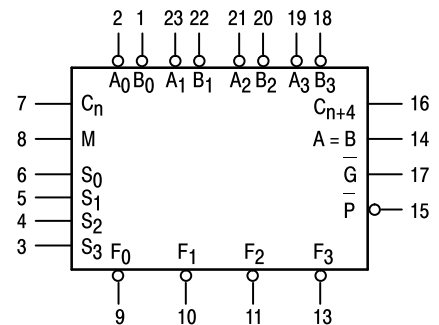


N SUFFIX  
PLASTIC  
CASE 649-03

### ORDERING INFORMATION

SN54LSXXXJ Ceramic  
SN74LSXXXN Plastic

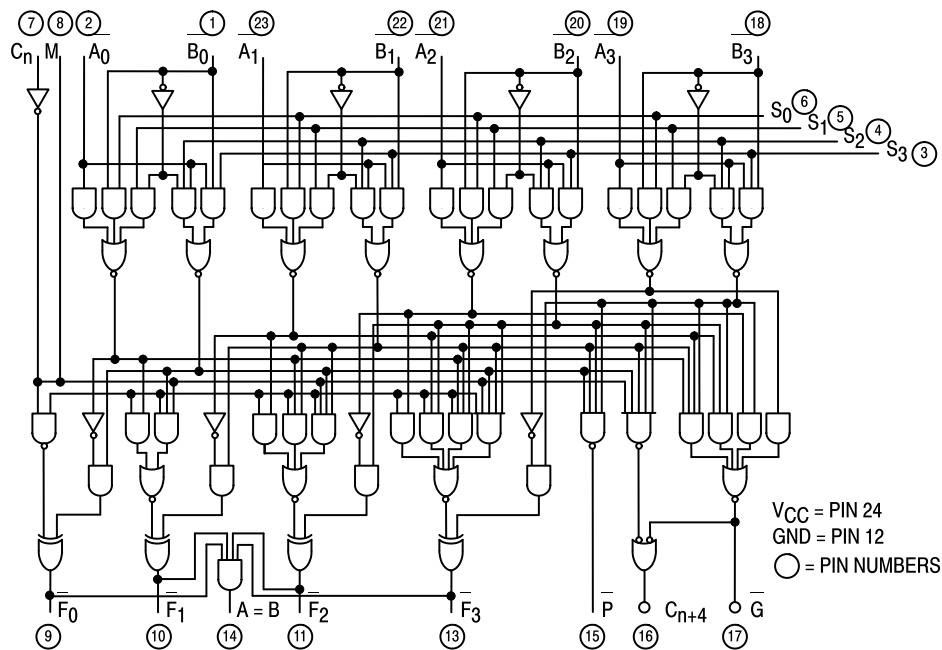
### LOGIC SYMBOL



$V_{CC}$  = PIN 24  
GND = PIN 12

# SN54/74LS181

## LOGIC DIAGRAM



## FUNCTIONAL DESCRIPTION

The SN54/74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ( $S_0 \dots S_3$ ) and the Mode Control Input ( $M$ ), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input ( $M$ ) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the  $C_{n+4}$  output, or for carry lookahead between packages using the signals  $P$  (Carry Propagate) and  $G$  (Carry Generate),  $P$  and  $G$  are not affected by carry in. When speed requirements are not stringent, the LS181 can be used in a simple ripple carry mode by connecting the Carry Output ( $C_{n+4}$ ) signal to the Carry Input ( $C_n$ ) of the next unit. For high speed operation the LS181 is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of the four LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability

over extremely long word lengths.

The  $A = B$  output from the LS181 goes HIGH when all four  $F$  outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The  $A = B$  output is open collector and can be wired-AND with other  $A = B$  outputs to give a comparison for more than four bits. The  $A = B$  signal can also be used with the  $C_{n+4}$  signal to indicate  $A > B$  and  $A < B$ .

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates  $A$  minus  $B$  minus 1 (2s complement notation) without a carry in and generates  $A$  minus  $B$  when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, the LS181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

# SN54/74LS181

FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
				LOGIC (M = H)	ARITHMETIC** (M = L) (C <sub>n</sub> = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C <sub>n</sub> = H)
S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>				
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	$\overline{AB}$ minus 1	$\overline{A + B}$	A + $\overline{B}$
L	L	H	L	A + $\overline{B}$	AB minus 1	AB	A + B
L	L	H	H	Logical 1 minus 1		Logical 0 minus 1	
L	H	L	L	$\overline{A + B}$	A plus (A + $\overline{B}$ )	$\overline{AB}$	A plus AB
L	H	L	H	$\overline{B}$	AB plus (A + B)	B	(A + B) plus AB
L	H	H	L	$A \oplus \overline{B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$\overline{A + B}$	A + B	$\overline{AB}$	AB minus 1
H	L	L	L	AB	A plus (A + B)	$\overline{A + B}$	A plus AB
H	L	L	H	$A \oplus B$	$\overline{A}$ plus B	$A \oplus B$	A plus $\overline{B}$
H	L	H	L	B	AB plus (A + B)	B	(A + B) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logical 0	A plus A*	Logical 1	A plus A*
H	H	L	H	AB	$\overline{AB}$ plus A	A + B	(A + $\overline{B}$ ) plus A
H	H	H	L	AB	AB plus A	A + B	(A + B) Plus A
H	H	H	H	A	A	A	A minus 1

L = LOW Voltage Level

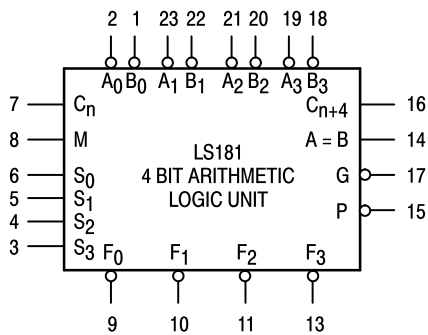
H = HIGH Voltage Level

\*Each bit is shifted to the next more significant position

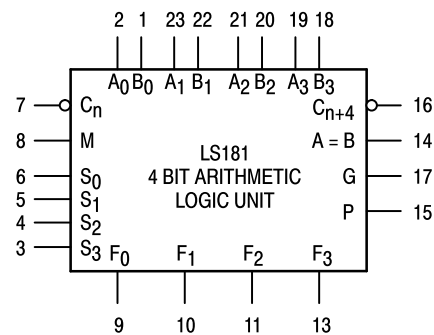
\*\*Arithmetic operations expressed in 2s complement notation

## LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T <sub>A</sub>	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
I <sub>OL</sub>	Output Current — Low	54			4.0	mA
		74			8.0	
V <sub>OH</sub>	Output Voltage — High (A = B only)	54, 74			5.5	V

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## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
$V_{IK}$	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
		74	2.7	3.5		V	
$V_{OL}$	Output LOW Voltage Except G and P	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
	Output $\bar{G}$	54, 74			0.7	V	$I_{OL} = 16 \text{ mA}$
	Output $\bar{P}$	54 74			0.6 0.5	V	$I_{OL} = 8.0 \text{ mA}$
$I_{OH}$	Output HIGH Current	54, 74			100	$\mu\text{A}$	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$I_{IH}$	Input HIGH Current Mode Input Any A or B Input Any S Input $C_n$ Input				20 60 80 100	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
	Mode Input Any A or B Input Any S Input $C_n$ Input				0.1 0.3 0.4 0.5	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current Mode Input Any A or B Input Any S Input $C_n$ Input				-0.4 -1.2 -1.6 -2.0	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 2)		-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current See Note 1A	54			32	mA	$V_{CC} = \text{MAX}$
		74			34		
	See Note 1B	54			35		
		74			37		

Note 1.

With outputs open,  $I_{CC}$  is measured for the following conditions:

A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

Note 2: Not more than one output should be shorted at a time, nor for more than 1 second.

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AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V}$ , Pin 12 = GND,  $C_L = 15\text{ pF}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay, ( $C_n$ to $C_{n+4}$ )		18 13	27 20	ns	$M = 0\text{ V}$ , (Sum or Diff Mode) See Fig. 4 and Tables I and II
$t_{PLH}$ $t_{PHL}$	( $C_n$ to $\bar{F}$ Outputs)		17 13	26 20	ns	$M = 0\text{ V}$ , (Sum Mode) See Fig. 4 and Table I
$t_{PLH}$ $t_{PHL}$	( $\bar{A}$ or $\bar{B}$ Inputs to $\bar{G}$ Output)		19 15	29 23	ns	$M = S_1 = S_2 = 0\text{ V}$ , $S_0 = S_3 = 4.5\text{ V}$ (Sum Mode) See Fig. 4 and Table I
$t_{PLH}$ $t_{PHL}$	( $\bar{A}$ or $\bar{B}$ Inputs to $\bar{G}$ Output)		21 21	32 32	ns	$M = S_0 = S_3 = 0\text{ V}$ , $S_1 = S_2 = 4.5\text{ V}$ (Diff Mode) See Fig. 5 and Table II
$t_{PLH}$ $t_{PHL}$	( $\bar{A}$ or $\bar{B}$ Inputs to $\bar{P}$ Output)		20 20	30 30	ns	$M = S_1 = S_2 = 0\text{ V}$ , $S_0 = S_3 = 4.5\text{ V}$ (Sum Mode) See Fig. 4 and Table I
$t_{PLH}$ $t_{PHL}$	( $\bar{A}$ or $\bar{B}$ Inputs to $\bar{P}$ Output)		20 22	30 33	ns	$M = S_0 = S_3 = 0\text{ V}$ , $S_1 = S_2 = 4.5\text{ V}$ (Diff Mode) See Fig. 5 and Table II
$t_{PLH}$ $t_{PHL}$	( $\bar{A}_X$ or $\bar{B}_X$ Inputs to $\bar{F}_X$ Output)		21 13	32 20	ns	$M = S_1 = S_2 = 0\text{ V}$ , $S_0 = S_3 = 4.5\text{ V}$ (Sum Mode) See Fig. 4 and Table I
$t_{PLH}$ $t_{PHL}$	( $\bar{A}_X$ or $\bar{B}_X$ Inputs to $\bar{F}_X$ Output)		21 21	32 32	ns	$M = S_0 = S_3 = 0\text{ V}$ , $S_1 = S_2 = 4.5\text{ V}$ (Diff Mode) See Fig. 5 and Table II
$t_{PLH}$ $t_{PHL}$	( $A_X$ or $B_X$ Inputs to $F_{XH}$ Outputs)			38 26	ns	$M = S_1 = S_2 = 0\text{ V}$ , $S_0 = S_3 = 4.5\text{ V}$ (Sum Mode) See Fig. 4 and Table I
$t_{PLH}$ $t_{PHL}$	( $A_X$ or $B_X$ Inputs to $F_{XH}$ Outputs)			38 38	ns	$M = S_0 = S_3 = 0\text{ V}$ , $S_1 = S_2 = 4.5\text{ V}$ (Diff Mode) See Fig. 5 and Table II
$t_{PLH}$ $t_{PHL}$	( $\bar{A}$ or $\bar{B}$ Inputs to $\bar{F}$ Outputs)		22 26	33 38	ns	$M = 4.5\text{ V}$ (Logic Mode) See Fig. 4 and Table III
$t_{PLH}$ $t_{PHL}$	( $\bar{A}$ or $\bar{B}$ Inputs to $C_{n+4}$ Output)		25 25	38 38	ns	$M = 0\text{ V}$ , $S_0 = S_3 = 4.5\text{ V}$ , $S_1 = S_2 = 0\text{ V}$ (Sum Mode) See Fig. 6 and Table I
$t_{PLH}$ $t_{PHL}$	( $\bar{A}$ or $\bar{B}$ Inputs to $C_{n+4}$ Output)		27 27	41 41	ns	$M = 0\text{ V}$ , $S_0 = S_3 = 0\text{ V}$ , $S_1 = S_2 = 4.5\text{ V}$ (Diff Mode)
$t_{PLH}$ $t_{PHL}$	( $\bar{A}$ or $\bar{B}$ Inputs to $A = B$ Output)		33 41	50 62	ns	$M = S_0 = S_3 = 0\text{ V}$ , $S_1 = S_2 = 4.5\text{ V}$ $R_L = 2.0\text{ k}\Omega$ (Diff Mode) See Fig. 5 and Table II

## AC WAVEFORMS

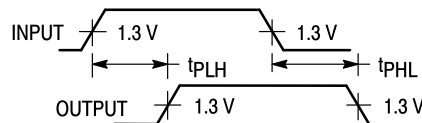


Figure 4

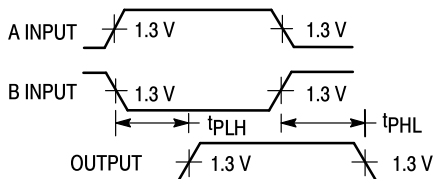


Figure 5

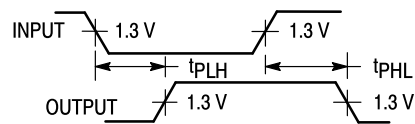


Figure 6

# SN54/74LS181

**SUM MODE TEST TABLE I**

**FUNCTION INPUTS:**  $S_0 = S_3 = 4.5\text{ V}$ ,  $S_1 = S_2 = M = 0\text{ V}$

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	
t <sub>PLH</sub> t <sub>PHL</sub>	$\bar{A}_i$	$\bar{B}_i$	None	Remaining A and B	C <sub>n</sub>	$\bar{F}_i$
t <sub>PLH</sub> t <sub>PHL</sub>	$\bar{B}_i$	$\bar{A}_i$	None	Remaining A and B	C <sub>n</sub>	$\bar{F}_i$
t <sub>PLH</sub> t <sub>PHL</sub>	$\bar{A}_i$	$\bar{B}_i$	None	C <sub>n</sub>	Remaining A and B	$\bar{F}_{i+1}$
t <sub>PLH</sub> t <sub>PHL</sub>	$\bar{B}_i$	$\bar{A}_i$	None	C <sub>n</sub>	Remaining A and B	$\bar{F}_{i+1}$
t <sub>PLH</sub> t <sub>PHL</sub>	$\bar{A}$	$\bar{B}$	None	None	Remaining A and B, C <sub>n</sub>	$\bar{P}$
t <sub>PLH</sub> t <sub>PHL</sub>	$\bar{B}$	$\bar{A}$	None	None	Remaining A and B, C <sub>n</sub>	$\bar{P}$
t <sub>PLH</sub> t <sub>PHL</sub>	$\bar{A}$	None	$\bar{B}$	Remaining B	Remaining A, C <sub>n</sub>	$\bar{G}$
t <sub>PLH</sub> t <sub>PHL</sub>	$\bar{B}$	None	$\bar{A}$	Remaining B	Remaining A, C <sub>n</sub>	$\bar{G}$
t <sub>PLH</sub> t <sub>PHL</sub>	$\bar{A}$	None	$\bar{B}$	Remaining B	Remaining A, C <sub>n</sub>	C <sub>n+4</sub>
t <sub>PLH</sub> t <sub>PHL</sub>	$\bar{B}$	None	$\bar{A}$	Remaining B	Remaining A, C <sub>n</sub>	C <sub>n+4</sub>
t <sub>PLH</sub> t <sub>PHL</sub>	C <sub>n</sub>	None	None	All A	All B	Any F or C <sub>n+4</sub>

# SN54/74LS181

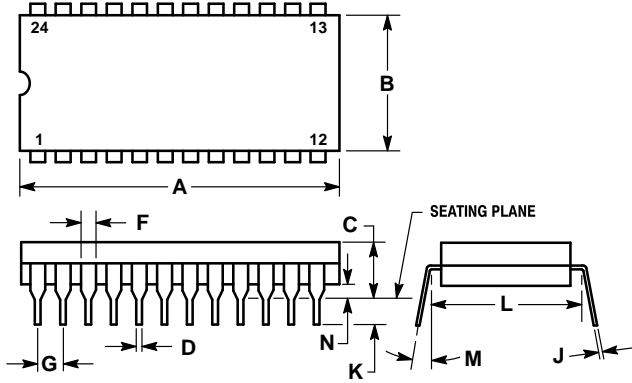
**DIFF MODE TEST TABLE II**
**FUNCTION INPUTS:  $S_1 = S_2 = 4.5\text{ V}$ ,  $S_0 = S_3 = M = 0\text{ V}$** 

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	
$t_{PLH}$ $t_{PHL}$	$\bar{A}$	None	$\bar{B}$	Remaining A	Remaining B, $C_n$	$\bar{F}_l$
$t_{PLH}$ $t_{PHL}$	$\bar{B}$	$\bar{A}$	None	Remaining A	Remaining B, $C_n$	$\bar{F}_l$
$t_{PLH}$ $t_{PHL}$	$\bar{A}_l$	None	$\bar{B}_l$	Remaining B, $C_n$	Remaining A	$\bar{F}_{l+1}$
$t_{PLH}$ $t_{PHL}$	$\bar{B}_l$	$\bar{A}_l$	None	Remaining B, $C_n$	Remaining A	$\bar{F}_{l+1}$
$t_{PLH}$ $t_{PHL}$	$\bar{A}$	None	$\bar{B}$	None	Remaining A and B, $C_n$	$\bar{P}$
$t_{PLH}$ $t_{PHL}$	$\bar{B}$	$\bar{A}$	None	None	Remaining A and B, $C_n$	$\bar{P}$
$t_{PLH}$ $t_{PHL}$	$\bar{A}$	$\bar{B}$	None	None	Remaining A and $B_l$ , $C_n$	$\bar{G}$
$t_{PLH}$ $t_{PHL}$	$\bar{B}$	None	$\bar{A}$	None	Remaining A and B, $C_n$	$\bar{G}$
$t_{PLH}$ $t_{PHL}$	$\bar{A}$	None	$\bar{B}$	Remaining A	Remaining B, $C_n$	A = B
$t_{PLH}$ $t_{PHL}$	$\bar{B}$	$\bar{A}$	None	Remaining A	Remaining B, $C_n$	A = B
$t_{PLH}$ $t_{PHL}$	$\bar{A}$	$\bar{B}$	None	None	Remaining A and B, $C_n$	$C_{n+4}$
$t_{PLH}$ $t_{PHL}$	$\bar{B}$	None	$\bar{A}$	None	Remaining A and B, $C_n$	$C_{n+4}$
$t_{PLH}$ $t_{PHL}$	$C_n$	None	None	All A and B	None	$C_{n+4}$

**LOGIC MODE TEST TABLE III**

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Function Inputs
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
$t_{PLH}$ $t_{PHL}$	$\bar{A}$	None	$\bar{B}$	None	Remaining A and B, $C_n$	Any $\bar{F}$	$S_1 = S_2 = M = 4.5\text{ V}$ $S_0 = S_3 = 0\text{ V}$
$t_{PLH}$ $t_{PHL}$	$\bar{B}$	None	$\bar{A}$	None	Remaining A and B, $C_n$	Any $\bar{F}$	$S_1 = S_2 = M = 4.5\text{ V}$ $S_0 = S_3 = 0\text{ V}$

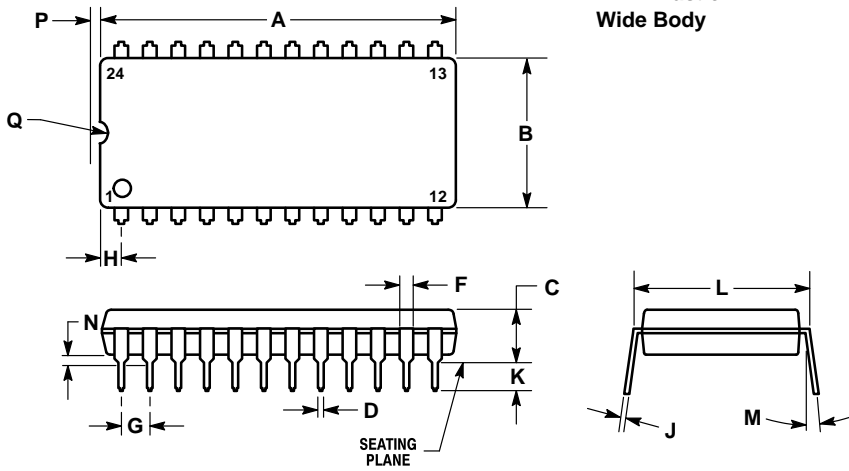
**Case 623-05 J Suffix  
24-Pin Ceramic Dual In-Line  
(WIDE BODY)**



- NOTES:
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050


**Case 649-03 N Suffix  
24-Pin Plastic  
Wide Body**



- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  - DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - 649-02 OBSOLETE, NEW STD 649-03 SEE ISSUE "C" FOR REFERENCE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030



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